WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a data memory having a plurality of memory regions to store data at addresses specified;

a code memory having the same address space as the data memory to store error correction codes for correcting each pieces of data that are stored in the memory regions of the data memory;

an error correction code control circuit including an error correction code generation circuit, a syndrome generation circuit and an error correction code decoding circuit, generating an error correction code for correcting data read from any memory region of the data memory before the data is written back into the memory region, and comparing the generated error correction code with an error correction code read from the code memory corresponding to the memory region, thereby to determine whether the data is erroneous and to correct the data when the data is erroneous; and

an error correction code function invalidity control circuit invalidating an error correction function of the error correction code control circuit for pieces of data read from the memory regions of the data memory when the memory regions are accessed first after power application.

2. The semiconductor memory according to claim 1, further comprising a memory cell array being accessed

simultaneously with the memory regions to store valid bits corresponding to the memory regions of the data memory, and in which valid bits are initialized into invalid state by a reset signal after power application,

wherein the error correction code function invalidity control circuit outputs a signal to stop the syndrome generation circuit when data is read from any memory region of the data memory, if the data stored in the memory cell corresponding to the memory region is an initial value; and

the error correction code control circuit controls to rewrite a valid bit into valid state in the memory cell corresponding to the memory region when data is first read from the memory region of the data memory after power application.

3. The semiconductor memory according to claim 2, wherein the memory cell array is added to the data memory.

4. The semiconductor memory according to claim 2, wherein the memory cell array comprises an initialization circuit connected to a pair of bit lines and a plurality of memory cells connected to word lines and the pair of bit lines, the word lines being connected commonly with the corresponding memory cells of the memory regions.

5. The semiconductor memory according to claim 3,

wherein the memory cell array comprises an initialization circuit connected to a pair of bit lines and a plurality of memory cells connected to word lines and the pair of bit lines, the word lines being connected commonly with the corresponding memory cells of the memory regions.

6. The semiconductor memory according to claim 4, wherein each of the memory cells of the memory cell array is selectively controlled by a word line commonly connected with each of corresponding memory cells of the data memory.

7. The semiconductor memory according to claim 5, wherein each of the memory cells of the memory cell array is selectively controlled by a word line commonly connected with each of the corresponding memory cells of the data memory.

8. The semiconductor memory according to claim 1, wherein the error correction code function invalidity control circuit automatically generates addresses corresponding to the memory regions of the data memory, pieces of initial data and pieces of code data corresponding to the pieces of initial data, and stops function of the error correction code control circuit immediately after power application before the error correction code control circuit writes the pieces of initial data into the corresponding memory regions of the data memory, and the pieces of code data into the

corresponding code memory, respectively.

9. The semiconductor memory according to claim 2, wherein the error correction code function invalidity control circuit automatically generates addresses corresponding to the memory regions of the data memory, pieces of initial data and pieces of code data corresponding to the pieces of initial data, and stops function of the error correction code control circuit immediately after power application before the error correction code control circuit writes the pieces of initial data into the corresponding memory regions of the data memory, and the pieces of code data into the corresponding code memory, respectively.

10. The semiconductor memory according to claim 3, wherein the error correction code function invalidity control circuit automatically generates addresses corresponding to the memory regions of the data memory, pieces of initial data and pieces of code data corresponding to the pieces of initial data, and stops function of the error correction code control circuit immediately after power application before the error correction code control circuit writes the pieces of initial data into the corresponding memory regions of the data memory, and the pieces of code data into the corresponding code memory, respectively.

11. The semiconductor memory according to claim 1, wherein the error correction code function invalidity

control circuit outputs a signal to stop the error correction code control circuit immediately after power application before the error correction code control circuit writes test pattern data into the memory regions of the data memory and the code data of the pattern data into the code memory.

12. The semiconductor memory according to claim 11, wherein the error correction code function invalidity control circuit is incorporated as part of a built-in self test circuit for use in initial testing.

13. A semiconductor memory comprising:

a data memory having a plurality of memory regions to store data at addresses specified;

a code memory having the same address space as the data memory to store error correction codes for correcting each pieces of data that are stored in the memory regions of the data memory;

an error correction code control circuit including an error correction code generation circuit, a syndrome generation circuit and an error correction code decoding circuit, generating an error correction code for correcting data read from any memory region of the data memory before the data is written back into the memory region, and comparing the generated error correction code with an error correction code read from the code memory corresponding to the memory region, thereby to determine whether the data is erroneous and

to correct the data when the data is erroneous;

an error correction code function invalidity control circuit invalidating an error correction function of the error correction code control circuit for pieces of data read from the memory regions of the data memory when the memory regions are accessed first after power application; and

a group of memory circuit being configured independently of the data memory to store valid bits corresponding to the memory regions of the data memory, being accessed simultaneously with the corresponding memory regions so that the valid bits stored are initialized by a resetting signal after power application,

wherein the error correction code function invalidity control circuit outputs a signal to stop the syndrome generation circuit when data is read from any memory region of the data memory, if the data stored in the memory cell corresponding to the memory region is an initial value; and

the error correction code control circuit rewrites a valid bit to valid state in the memory cell corresponding to the memory region when data is first read from the memory region of the data memory after power application.

14. The semiconductor memory according to claim 13, wherein the memory cell array comprises

an initialization circuit connected to a pair of bit lines and a plurality of memory cells connected to word lines and the pair of bit lines, the word lines connecting the corresponding memory cells in the data memory and the memory cell array.

15. The semiconductor memory according to claim 14, wherein each of the memory cells of the memory cell array is selectively controlled by a word line commonly connected with each of the corresponding memory cells of the data memory.

16. The semiconductor memory according to claim 13, wherein the error correction code function invalidity control circuit automatically generates addresses corresponding to the memory regions of the data memory, pieces of initial data and pieces of code data corresponding to the pieces of initial data, and stops function of the error correction code control circuit immediately after power application before the error correction code control circuit writes the pieces of initial data into the corresponding memory regions of the data memory, and the pieces of code data into the corresponding code memory, respectively.

17. The semiconductor memory according to claim 14, wherein the error correction code function invalidity control circuit automatically generates addresses corresponding to the memory regions of the data memory, pieces of initial data and pieces of code

data corresponding to the pieces of initial data, and stops function of the error correction code control circuit immediately after power application before the error correction code control circuit writes the pieces of initial data into the corresponding memory regions of the data memory, and the pieces of code data into the corresponding code memory, respectively.

18. The semiconductor memory according to claim 13, the error correction code function invalidity control circuit outputs a signal to stop the error correction code control circuit immediately after power application before the error correction code control circuit writes test pattern data into the memory regions of the data memory and the code data of the pattern data into the code memory.

19. The semiconductor memory according to claim 13, wherein the error correction code function invalidity control circuit is incorporated as part of a built-in self test circuit for use in initial testing.

20. A semiconductor memory comprising:

a data memory having a plurality of memory regions to store data at addresses specified;

a code memory having the same address space as the data memory to store error correction codes for correcting each pieces of data that are stored in the memory regions of the data memory;

an error correction code control circuit including an error correction code generation circuit, a syndrome generation circuit and an error correction code decoding circuit, generating an error correction code for correcting data read from any memory region of the data memory before the data is written back into the memory region, and comparing the generated error correction code with an error correction code read from the code memory corresponding to the memory region, thereby to determine whether the data is erroneous and to correct the data when the data is erroneous; and

a built-in self test circuit including a self-test function, a data memory initialization function and an error correction code function invalidity control function and being connected to a syndrome generation circuit and an error correction code decoding circuit in an error correction code control circuit to realize the error correction code function invalidity control function,

wherein the error correction code function invalidity control function of the built-in self test circuit invalidates an error correction function on the data read from the memory regions controlled by the error correction code control circuit when the memory regions of the data memory are accessed first after power application.